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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,581	03/17/2004	Andrew Marshall	TI-37089	6141

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,581	MARSHALL ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-10* is/are rejected.

7)☒ Claim(s) *5,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsunezawa (USP 6249174).

As to claim 1, Tsunezawa discloses in figure 5 a circuit for turning on an internal voltage rail (at drain of M17) comprising: a first transistor (M17) coupled between a power supply node (Vdd) and an internal voltage rail node (Va); a second transistor (M9) coupled to a control node of the first transistor; a third transistor (M12) coupled to the second transistor and having control node coupled to the control node the first transistor; a fourth transistor (M11) coupled between the second transistor and the power supply node; and a fifth transistor (M13) coupled between the third transistor and the power supply node, wherein the third transistor is coupled between the second transistor and the fifth transistor.

As to claim 2, figure 5 shows that the first, second, third, fourth, and fifth transistors are MOS transistors.

As to claim 3, figure 5 shows that the first, third, fourth, and fifth transistors are a first conductivity type (P type), and the second transistor is a second conductivity type (N-type).

As to claim 4, figure 5 shows that the first, third, fourth, and fifth transistors are PMOS transistors, and the second transistor is an NMOS transistor.

As to claim 6, figure 5 shows internal circuitry (M18) coupled to the internal voltage rail node.

As to claim 7, figure 5 shows a first input node coupled to a control node of the second transistor; a second input node coupled to a control node of the fourth transistor; and a third input node coupled to a control node fifth transistor.

3. Claims 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi (USP 6163206).

As to claim 8, Kobayashi discloses in figure 1, method for turning on an internal voltage rail (Vbias) comprising: coupling a first transistor (P3) between a power supply node (Vdd) and an internal voltage rail node; mirroring a current from a second transistor (P2) to the first transistor during a turn-on time period (from t1 to t2 shown in figure 4B); and coupling (by using transistor N4) a control node of the first transistor to a bias voltage node after the turn-on time period (from t2 to t7).

As to claim 9, figure 1 shows that the bias voltage node is a ground node.

As to claim 10, figure 1 shows the step of coupling a third transistor (N4) between the second transistor and the bias voltage node for coupling the control node of the first transistor to the bias voltage node.

Allowable Subject Matter

4. Claims 5, 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 5 would be allowable because the prior art fails to teach or suggest a first inverter coupled to a control node of the fourth transistor; a second inverter coupled to a control node of the fifth transistor; and a buffer coupled to a control node of the second transistor.

Claims 11 and 12 would be allowable because the prior art fails to teach or suggest the step of coupling a fourth transistor between the second transistor and the power supply node, wherein the fourth transistor is turned on during the turn-on time period and turned off after the turn-on time period.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

May 31, 2005